### Getting Started with TDSHT3

You can use this side of the Quick Reference Card to get started with the Source Clock-Data Tests Select All test procedure. The other side contains a complete menu tree for the TDSHT3 HDMI Compliance Test Software.

NOTE. For additional procedures, refer to the Quick Start User Manual. For complete operating instructions, refer to the Online

**TDSHT3 HDMI Compliance Test Software enables** unprecendented efficiency by providing a comprehensive range of tests, including Jitter Tolerance.

#### **Source Clock-Data Tests Select All**

This option enables you to run the eye diagram, duty cycle, rise time, fall time, clock jitter, over/undershoot v-h, over/undershoot v-l, and inter-pair skew test simultaneously.

You will need one supported oscilloscope, two differential probes, one DC power supply 3.3 V, one EDID emulator, and one TPA-P-DI fixture.

#### **Follow these steps:**

- 1. On the menu bar, click Tests > Select > Source.
- 2. In the clock-data tests pane, click Select All.



To change the configuration settings, click **Tests** > Configure. For most tests, you can use the factory default configuration. However, you can change the values by using the virtual keyboard or the general purpose knob on the oscilloscope front panel. Using the File menu, you can also restore the factory defaults or save and recall your own configuration settings.



For up-to-date information on Tektronix oscilloscope

solutions for HDMI Compliance Test Software, access

This software supports the TDS7254/B, TDS7404/B,

CSA7404/B, and TDS7704B series of oscilloscopes. Refer

to the Optional Applications Software on Windows-Based Oscilloscopes Installation Manual for a list of specific

models. The applications CD includes a PDF file of the

the www.tektronix.com Web page.

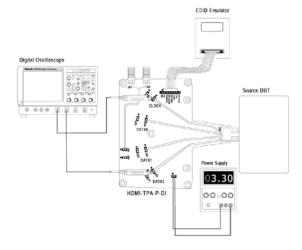
**TDSHT3 Ordering Information** 

online help.

4. To connect the DUT, click Tests > Connect.



5. Make the connections as follows:



**6.** Ensure that your signal in the oscilloscope display is similar to the sample signal. Click **View Waveform** to display a sample of the expected signal. If the displays are not similar, go back and check your configuration and connections.



Click **Run Test** to perform the test. The TDSHT3 **HDMI Compliance Test Software sets up the** oscilloscope and the test runs displaying a progress indicator.

To order along with oscilloscope:

- Opt. HT3 HDMI Compliance Test Software To order an upgrade for an existing oscilloscope:
- TDS7000/B Order TDS7UP/7BUP Opt. HT3
- CSA7000/B Order TDS7UP/7BUP Opt. HT3

# **Recommended Accessories**

## **Oscilloscopes**

- 16M Record Length/Ch Opt. 4M or more (for Eye Diagram and Jitter tests)
- Serial Trigger Opt. ST (for Inter-pair Skew tests)

## **HDMI Pattern Sources**

- Jitter Generation AWG710B (for Sink tests)
- Test Pattern Generation DTG 5274 and DTGM30 for Sink Tests (three required)

## **TDR Tests**

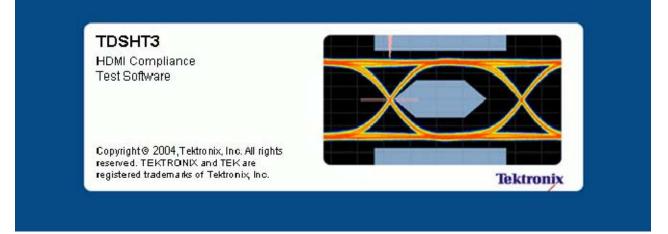
Oscilloscope - TDS8000B with 80E03 and 80E04

## **Probes**

- Differential Probes P6330, P7330 and P7350 (two probes required)
- Active Probes P7240 and above (two probes required)
- Probe Positioner PPM100 Flexible Arm Probe Posi-

## **Test Fixtures**

- Plug type HDMI TPA-P adapter set 013-A013-50
- Receptacle type HDMI TPA-R adapter set -013-A012-50



**8.** If you have run the tests successfully, the software makes Result available automatically and displays the eye diagram plot and the clock jitter plot. You can also view both the result summary of the test and the report configuration in the result pane.



9. In the result summary pane, click Result Details to display the results of the tests.

Test Name	Spec Range	Meas Value	Result	Remails/Comments			
7-9: Clock Jitter: CK	Clock Jitter < 0.25°Tbit:  Data Jitter < 0.3°Tbit:	0.004°TER 0.02°TER	Pass	Tbit = 1.5004ns; Vs = 690.92mV; Margin = 0.2671bit; Record Length = 0.0000c; Tbit = 1.5004ns; VsD = 510.08mV; Margin = 0.2671bit; Record Length = 0.0000c; Mark Hits = 0.			
7-10: Source Eye Diagram: CK							
7-6: Inter-Pair Skeut CK, D	Skew < 0.2*TPhoel;	0.0°TPbsel		Tbit = 1.5384ns; VsCK = 898.32mV; VsD = 515.05mV; Margin = 0.2*TPbv4t;	ı		
7-8: Max Duty Cycle: CK	Max Duty Cyole < 60.0%;	50.0%	Pass	Tbit = 1.5384ns; Margin = 10.0%;	1		
7-8: Min Duty Cycle: CK	40.0% < Min Duty Cycle:	49.35%	Pass	Tbit = 1.5394ns; Margin = 0.35%;	l.		
7-4: RiseTime: CK	76.00ss < TRISE < 615	128.00ps	Pass	Thit = 1,5984ns; Vs = 698,32mV; Upper Margin :	1		

10. In the Result Details dialog box, click Result Statistics to display statistics based on the tests.

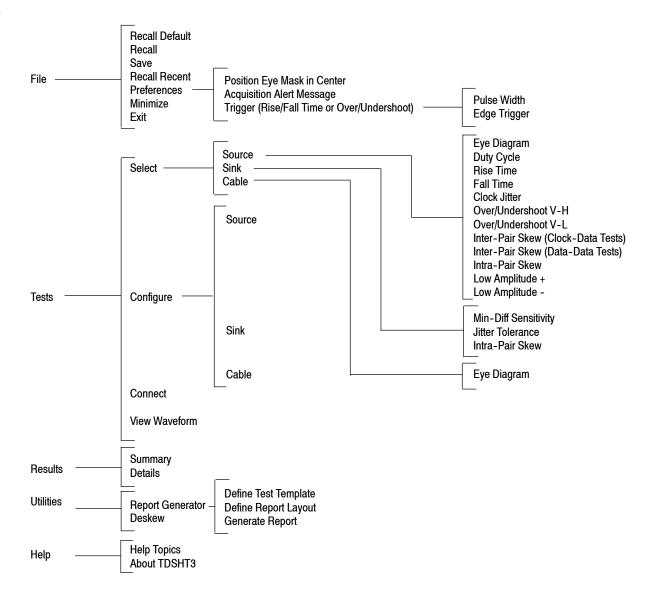
Test Name	Population	Min	Maic	Mean	Std Dev	Ph-Pk
7-9: Clock Jitter Tx Clock TIE: CK	52,000	-21.13	12.480ps	0.00s	7.9029ps	33.816
7-9: Clock Jitter Recovered Cloc	52.000	9.224	5.1142ps	3.755	3.6109ps	14.339
7-10: Source Eye Diagram Tx Cl	52,000	-21.13	12.400ps	0.00s	7.9029ps	33.616
7-10: Source Eye Diagram Reco	52 000	9.224	5.1142ps	3.755	3.6100ps	14,339
7-4: Rise Time: CK	661.95k	127.15ps	128.43ps	128.00ps	387.376	1.2843
7-4: Rise Time: D	990.54k	430.29ps	432.95ps	430.95ps	552.07ts	2.6550
7-4: Fall Time: CK	662.78k	104.12ps	106.02ps	104.39ps	418.60E	1.0065
7-4: Fall Time: D	896.58k	434.74ps	438.05ps		704.15ts	

The software calculates statistics for each selected test, and logs the statistics on a cycle-by-cycle basis in a fairly large waveform. The standard statistics are for the Maximum, Minimum, Mean, Standard Deviation, and Population.

**HDMI Compliance Test Software Source Test** 

## www.tektronix.com

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